UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,962	12/04/2003	Kwang-Wook Lee	8021-34 DIV (SS-14532-US)	7392

22150 7590 01/26/2006

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
UMEZ ERONINI, LYNETTE T	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 01/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,962	LEE ET AL.	
	Examiner	Art Unit	
	Lynette T. Umez-Eronini	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 10 and 13-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Belcher et al. (US 5,520,299) in view of Morinaga (US 6,143,705).

As to claims 10 and 14-16, Belcher teaches removal of BST surface damage or defects **44** and **46** by using a solvent etch that may include H_2O and a wet etch that may include: hydrofluoric acid and acetic (Table 2 [column 3, lines 39-24] and column 3, lines 47-58). Belcher also teaches cleaning from 30 seconds to 30 minutes (column 8, lines 1-18). The aforementioned reads on,

A method of selectively removing a damaged portion of a ferroelectric layer with a cleaning solution, the method comprising: providing an integrated circuit substrate having an exposed ferroelectric layer with the damaged portion; and selectively removing a damaged portion of the exposed ferroelectric layer with a cleaning solution by contacting the exposed ferroelectric layer with the cleaning solution, said cleaning solution including a fluoride, an organic acid with carboxyl group, and water, **in claim 10**;

wherein the fluoride is hydrogen fluoride, hydrocarbon tetrafluoride or ammonium fluoride, **in claim 14**;

wherein the organic acid is formic acid, acetic acid or citric acid, **in claim 15**; and

wherein the alkaline pH adjusting agent is ammonium hydroxide, potassium hydroxide, tetramethylammonium hydroxide or tetraethylammonium hydroxide, **in claim 16**.

Belcher differs in failing to teach removing a damaged portion of a ferroelectric layer with a cleaning solution that comprises an alkaline pH adjusting agent, **in claim 10**;

wherein the pH of the cleaning solution is about 4.5 to about 6.0, in **claim 13**;

wherein the content of the fluoride is about 0.01% to about 1% by weight based on the total weight of the cleaning solution, **in claim 17**;

wherein the content of the organic acid with carboxyl group is about 1% to about 50% by weight based on the total weight of the cleaning solution **in claim 18**; and

wherein the content of the alkali pH adjusting agent is about 0.25% to about 15% by weight based on the total weight of the cleaning solution **in claim 19**.

Morinaga teaches a method of treating (such as cleaning, [column 3, lines 62-65]) a substrate with a surface treatment composition (column 1, lines 5-7) that contains at least one of the following complexing agents: carboxylic acids such as acetic acid and hydrogen halides: such as hydrofluoric acid. The composition also comprises an alkaline aqueous solution having a pH of higher than 7 and including potassium hydroxide, tetramethyl ammonium hydroxide and the like (column 5, lines; column 5, lines 28-34 and 46-48, and column 6, lines 21-33). The complexing agent is present in a amount of 10^{-7} to 2 wt % (column 5, lines 55-62) and the alkaline solution is present in an amount of 0.01 to 30 wt % (column 6, lines 32-35), which encompasses content of the fluoride, organic acid and alkali pH adjusting agent, as specified **in claims 17-19**.

Morinaga illustrates cleaning a substrate with a composition comprising an alkaline solution, a fluoride, and an organic acid, having a concentration, which encompasses applicants' specifically claimed wt % and having a pH, which encompasses applicants' specifically claimed pH is known. Hence, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Belcher's cleaning method by using an alkaline solution as taught by Morinaga for the purpose of cleaning a semiconductor substrate without being contaminated with particles, organic materials, and metals (Morinaga, column 7, lines 49-57).

4. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Belcher et al. (US '299) in view of Morinaga (US '705) as applied to claim 1 above, and further in view of Applicants' admitted prior art).

Belcher in view of Morinaga differ in failing to disclose wherein the exposed ferroelectric layer includes a surface of the ferroelectric layer passed through annealing after deposition on the integrated circuit substrate, and the step of contacting the exposed ferroelectric layer with said cleaning solution includes etching back the ferroelectric layer from the top of the ferroelectric layer, **in claim 11**; and wherein the exposed ferroelectric layer is interposed between upper and lower electrode layers, and the method further comprises forming a capacitor by patterning the upper electrode layer, the ferroelectric layer and the lower electrode layer, before contacting the exposed ferroelectric layer with the cleaning solution, **in claim 12**.

Applicants' admitted prior art discloses manufacturing a FRAM capacitor (Discussion of Related Art, page 2, lines 10-25), which reads on the exposed ferroelectric layer includes a surface of the ferroelectric layer passed through annealing after deposition on the integrated circuit substrate, and the step of contacting the exposed ferroelectric layer with a cleaning solution includes etching back the ferroelectric layer from the top of the ferroelectric layer, **in claim 11**; and wherein the exposed ferroelectric layer is interposed between upper and lower electrode layers, and the method further comprises forming a capacitor by patterning the upper electrode layer, the ferroelectric layer and the lower electrode layer, before contacting the exposed ferroelectric layer with a cleaning solution, **in claim 12**.

Since Applicants' admitted prior art illustrates a method of manufacturing a capacitor is known, then it would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the cleaning solution of Belcher and Morinaga in cleaning a capacitor as disclosed in Applicants' admitted prior art because such structure is known in the manufacture of semiconductor devices.

Further since the combination of Applicants' admitted prior art and Belcher and Morinaga teaches cleaning a capacitor, then using the said combination as claimed by applicants would result in said cleaning solution includes etching back the ferroelectric layer by about 100 Å to about 500 Å.

5. Claims and 20, 23, 24, 27, 28, 29-33 rejected under 35 U.S.C. 103(a) as being unpatentable over Belcher in view of Morinaga.

Belcher in view of Morinaga differs in failing to teach wherein the organic acid dissolves a reduced metallic component of the ferroelectric layer, **in claim 20.**

Since the combination of Belcher and Morinaga teaches applicants method and cleaning composition, then using the said combination in the same manner as claimed by applicants would result wherein the organic acid dissolves a reduced metallic component of the ferroelectric layer.

6. Claims 21, 22, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Belcher (US '299) in view of Morinaga (US '706) as applied to claim 20 above, and further in view of Applicants' admitted prior art.

Belcher in view of Morinaga differs in failing to teach depositing and annealing the ferroelectric layer prior to selectively removing the damage portion of the ferroelectric layer, **in claim 21**;

wherein the step of selectively removing the damage portion of the ferroelectric layer includes removing a semi-stable pyrochlore structure that appears from a top portion of the ferroelectric layer, **in claim 22**;

wherein the exposed ferroelectric layer includes a surface of the ferroelectric layer passed through annealing after deposition on the integrated circuit substrate, and the step of contacting the exposed ferroelectric layer with said cleaning solution includes etching back the ferroelectric layer from a top portion of the ferroelectric layer, **in claim 25**; and

wherein the exposed ferroelectric layer is interposed between upper and lower electrode layers, and the method further comprises forming a capacitor by patterning the upper electrode layer, the ferroelectric layer and the lower electrode layer, before contacting the exposed ferroelectric layer with said cleaning solution, **in claim 26**.

Applicants' admitted prior art discloses manufacturing a FRAM capacitor and cleaning byproducts that result from etching electrode material or ferroelectric materials and that also damage the ferroelectric materials (Discussion of Related Art, page 2, lines 10-25), which reads on depositing and annealing the ferroelectric layer prior to selectively removing the damage portion of the ferroelectric layer, **in claim 21**; selectively removing the damage portion of the ferroelectric layer includes removing a semi-stable pyrochlore structure that appears from a top portion of the ferroelectric

layer, **in claim 22**; wherein the exposed ferroelectric layer includes a surface of the ferroelectric layer passed through annealing after deposition on the integrated circuit substrate, and the step of contacting the exposed ferroelectric layer with a cleaning solution includes etching back the ferroelectric layer from the top of the ferroelectric layer, **in claim 25**; and wherein the exposed ferroelectric layer is interposed between upper and lower electrode layers, and the method further comprises forming a capacitor by patterning the upper electrode layer, the ferroelectric layer and the lower electrode layer, before contacting the exposed ferroelectric layer with a cleaning solution, **in claim 26**.

Since Applicants' admitted prior art illustrates a method of manufacturing a ferroelectric capacitor and cleaning byproducts from the manufacturing method is known, then it would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the cleaning solution of Belcher and Morinaga in cleaning a capacitor as disclosed in Applicants' admitted prior art because such structure is know in the manufacture of semiconductor devices.

Further since the combination of Applicants' admitted prior art and Belcher and Morinaga teaches cleaning a capacitor, then using the said combination as claimed by applicants would result in removing a semi-stable pyrochlore structure that appears form a tip portion of the ferroelectric layer to a predetermined depth and said cleaning solution includes etching back the ferroelectric layer by about 100 Å to about 500 Å.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 571-272-1470. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Art Unit 1765

ltue

January 16, 2006

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER